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Asymmetric Electrical Properties of Half Corbino Hydrogenated Amorphous Silicon Thin-Film Transistor and Its Applications to Flat Panel Displays

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The half-Corbino hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) were fabricated with a five-photomask process used in the processing of the active matrix liquid-crystal displays (AM-LCD). We showed that the a-Si:H half-Corbino TFTs have the asymmetric electrical characteristics under different drain-bias conditions. In comparison to half-Corbino TFT with unpatterned gate electrode, the device parasitic capacitance can be significantly reduced by patterning the gate electrode for same device dimension, while the sub-threshold swing and threshold voltage remain identical for same bias condition. The OFF-current remains below 0.1 pA for all device configurations. Finally, we discuss their potential applications as a driving or switching TFT to various flat panel displays. © 2011 The Japan Society of Applied Physics

1. Introduction

Interdigitated electrodes were first adapted to achieve a high device width (W) to length (L) ratios in a limited layout space in metal oxide semiconductor field-effect transistors (MOSFET).[1,2] Organic thin-film transistors (OTFTs) also employed these structures to increase ON-current characteristics,[3,4] while bi-polar power transistors have generally used comb-like contact electrodes to minimize current crowing.[5] Recently, the comb-shaped electrodes have been also used in field-effect hydrogenated amorphous silicon (a-Si:H) solar cells to enhance the output power.[6] In a-Si:H TFT, one pair of interdigitated, so-called fork-shaped electrode was introduced to reduce a gate-to-source capacitance and a photo-leakage current that are critical for high-resolution active-matrix liquid crystal displays (AM-LCDs).[7,8]

Previously we reported the design and asymmetric electrical properties of a fork-shaped a-Si:H TFT with single interdigitated electrode[9] which has been used in AM-LCDs. Due to its unique geometry, we showed that a very low gate-to-pixel capacitance can be achieved in such device configurations. This reduction is desirable property for switching transistor used in AM-LCDs. However, at the same time, because of the small source electrode, the fork-shaped TFT's ON-current level is rather small in comparison to standard TFT. This can present its use as a driving TFT in active-matrix organic light-emitting displays (AM-OLEDs).

In this paper, first, we fabricated two types of half-Corbino a-Si:H TFTs and report on their asymmetric electrical characteristics. We showed that the gate-to-source parasitic capacitance (C_{GS}) of the device can be minimized by patterning the gate electrode. Then, we discuss their potential applications to AM-LCDs as switching TFT and to AM-OLEDs as switching and driving TFTs. To our best knowledge, this paper describes the first investigation of the half-Corbino a-Si:H TFTs' asymmetric electrical characteristics and their possible application to flat panel displays.

2. Half-Corbino a-Si:H TFT Fabrication

The half-Corbino a-Si:H TFT is consisting of rod-shaped inner electrode ($R_1 = 5\,\mu m$) and U-shaped outer electrode ($R_2 = 11\,\mu m$) as shown in Fig. 1. Bottom gate electrode is defined as (a) unpatterned electrode that is large enough to cover the entire device area of outer and inner electrodes; (b) patterned electrode that is large enough to cover only the device channel area with a 1 μm overlap between outer and inner electrodes. Both half-Corbino a-Si:H TFTs were fabricated using the normal AM-LCD five-photomask process steps.[10] More specifically, on the Corning Eagle2000 glass substrate, bi-layer of molybdenum (Mo, 500 Å) and aluminum–neodymium alloy (AlNd, 2000 Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet-etching (Mask 1). Following gate electrode definition, hydrogenated amor-

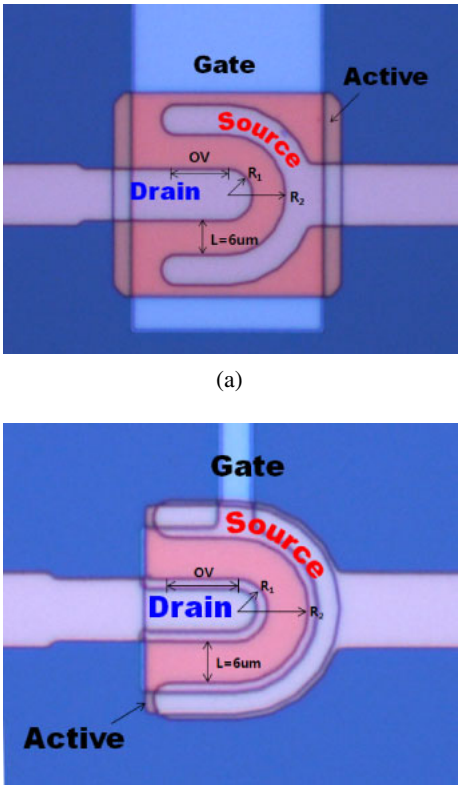

Fig. 1. (Color online) Top views of half Corbino TFT with (a) unpatterned gate electrode and (b) patterned gate electrode.

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phous silicon nitride (a-SiN$_x$:H, 4000 Å)/a-Si:H (1700 Å)/ phosphor-doped a-Si:H (n$^+$ a-Si:H, 300 Å) tri-layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to form gate insulator and active channel layer, respectively. After defining the device active island by reactive ion etching (RIE) (Mask 2), a chromium (Cr, 1200 Å) layer was deposited by sputtering, and source/drain (S/D) electrodes were patterned by wet-etching (Mask 3). Using S/D metal and photo resist as masks, the back-channel-etching by RIE was performed. Then, we deposited a-SiN$_x$:H (3000 Å) as a passivation (PVX) layer by PECVD at 300 °C. To realize an electrical contact to electrodes (source/drain and gate), vias were formed through the PVX layer by RIE (Mask 4). After contact vias definition, indium tin oxide (ITO, 500 Å) was deposited by a sputtering method at room temperature, and then pixel electrodes and probing pads were patterned by wet-etching (Mask 5). As a final step, the thermal annealing was performed for an hour at 235 °C in the air. Figure 2 shows the cross-sectional views of fabricated half-Corbino a-Si:H TFTs with (a) unpatterned and (b) patterned gate electrodes; PVX and ITO pixel electrodes are not shown in these figures for clarity.

3. Experimental Results

To characterize the electronic properties of half-Corbino a-Si:H TFTs, we first measured the device output characteristics as shown in Fig. 3, by applying the drain to source bias (V_{DS}) under following conditions: (1) ground was applied on the outer U-shaped source electrode and drain voltage was applied on the inner rod-shaped drain electrode; (2) drain voltage was applied on the outer U-shaped drain electrode and ground was applied on the inner rod-shaped source electrode. We swept the drain bias from 0 to 20 V for various gate to source voltages (V_{GS} = 0, 10, and 20 V). As shown in Fig. 3(a) for the half-Corbino TFT with unpatterned gate electrode, at V_{DS} = 20 V and V_{GS} = 20 V, the output current for condition (1) (= 8.6 μA) is 1.24 times higher than for condition (2) (= 7.0 μA). However, as shown in Fig. 3(b) for the half-Corbino TFT with patterned gate electrode, the output currents decrease to 7.0 and 5.3 μA for condition (1) and (2), respectively, for the same V_{DS} and V_{GS} values.

Next, we measured the transfer characteristics with unpatterned gate electrode; we swept the gate bias from 25 to 0 V, and swept again from 0 to 25 V for various drain voltages (0.1, 10, and 20 V). As shown in Fig. 4(a), at low drain voltage (V_{DS} = 0.1 V), the ON-currents are identical for both bias conditions. However, at high V_{DS} (> 10 V), the ON-currents for case (1) are higher than for case (2). Therefore, regardless of gate bias and direction of drain bias applied, the ON-currents would be the same for a low drain bias. However, when we apply a high drain bias, the ON-current levels can be significantly increased depending on the drain-bias direction. However, at the same time, as the drain bias is increased from 0.1 to 10 V, the OFF-currents for both condition (1) and (2) showed identical behavior regardless of drain biases; they increased from $\sim 10^{-14}$ to $\sim 10^{-13}$. Then we repeated the same measurement for half-Corbino a-Si:H TFT with patterned gate electrode as shown in Fig. 4(b). We observed the same behavior as one described above for unpatterned gate electrode. During gate bias sweeping, both types of transistors do not show

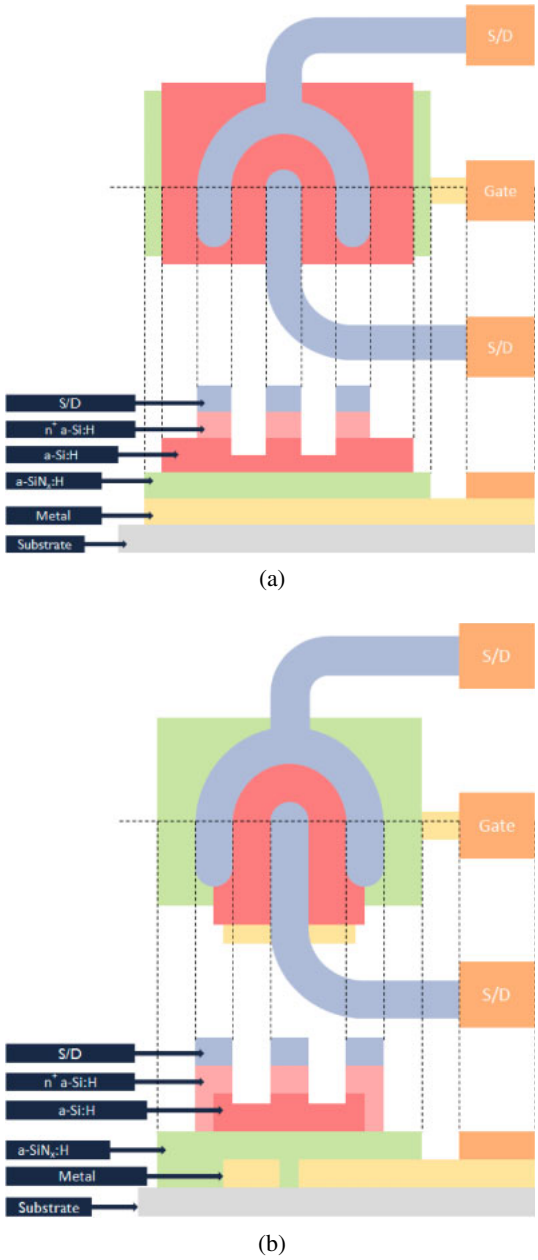


Fig. 2. (Color online) Cross-sectional views of half Corbino TFT with (a) unpatterned gate electrode and (b) patterned gate electrode.

any significant hysteresis (ΔV_{GS}) in current–voltage characteristics for both bias conditions; at V_{DS} = 10 V and I_{DS} = 0.1 nA, both cases showed ΔV_{GS} = 0.5 V for condition (1) and 0.46 V for condition (2), which is acceptable for AM-LCDs.

4. Definitions of a-Si:H Half-Corbino TFT Geometrical Factor

From previous observations on Corbino a-Si:H TFTs[11] and fork-shaped a-Si:H TFTs,[9] it is known that the asymmetric behaviors of half-Corbino a-Si:H TFT described above can be explained by varying effective channel width and length (geometric factor) of a-Si:H TFT depending on the source and drain bias conditions. For the different bias conditions, the geometric factor of half Corbino a-Si:H TFT can be defined in a similar way for linear and saturation regime operation to extract the device electrical parameters.

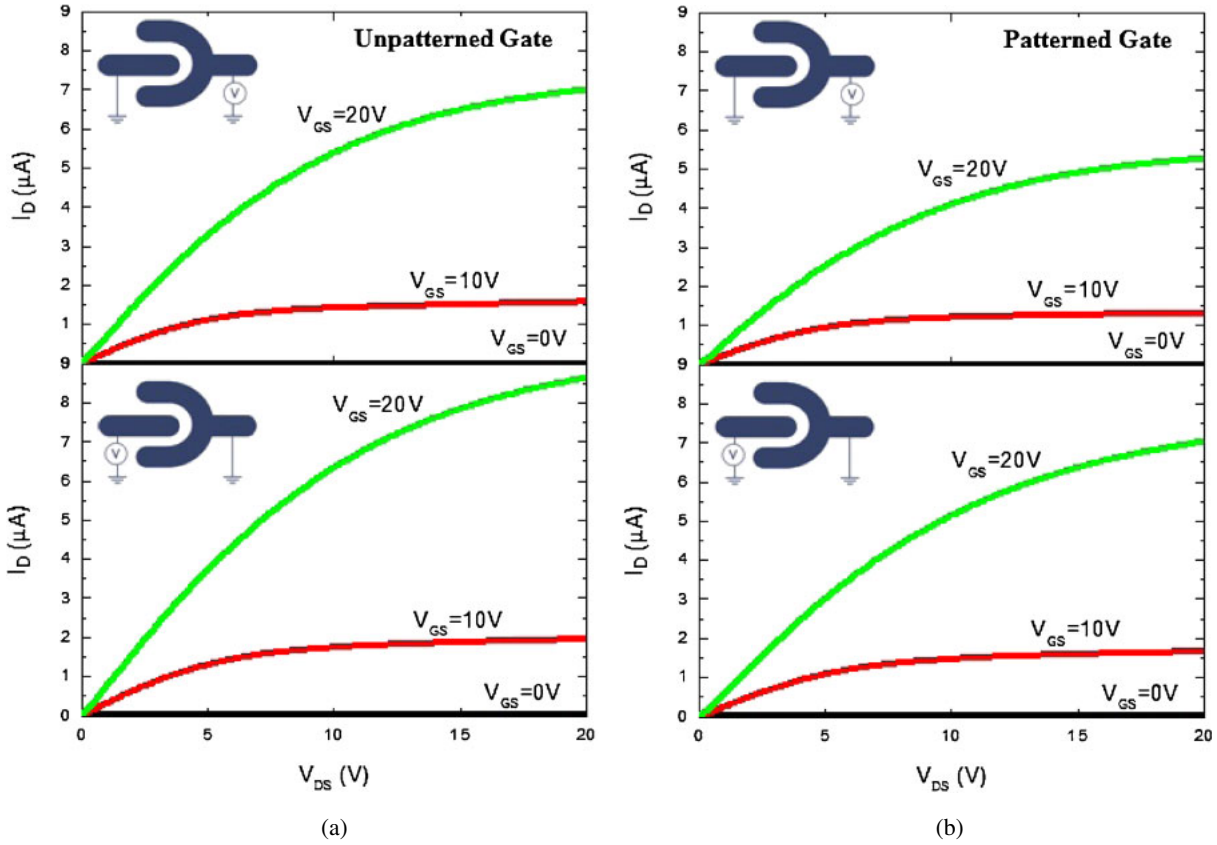


Fig. 3. (Color online) Asymmetric output characteristics of half Corbino a-Si:H TFTs with $L = 6\,\mu m$ and $OV = 6\,\mu m$ for different source bias conditions: (a) unpatterned gate electrode and (b) patterned gate electrode.

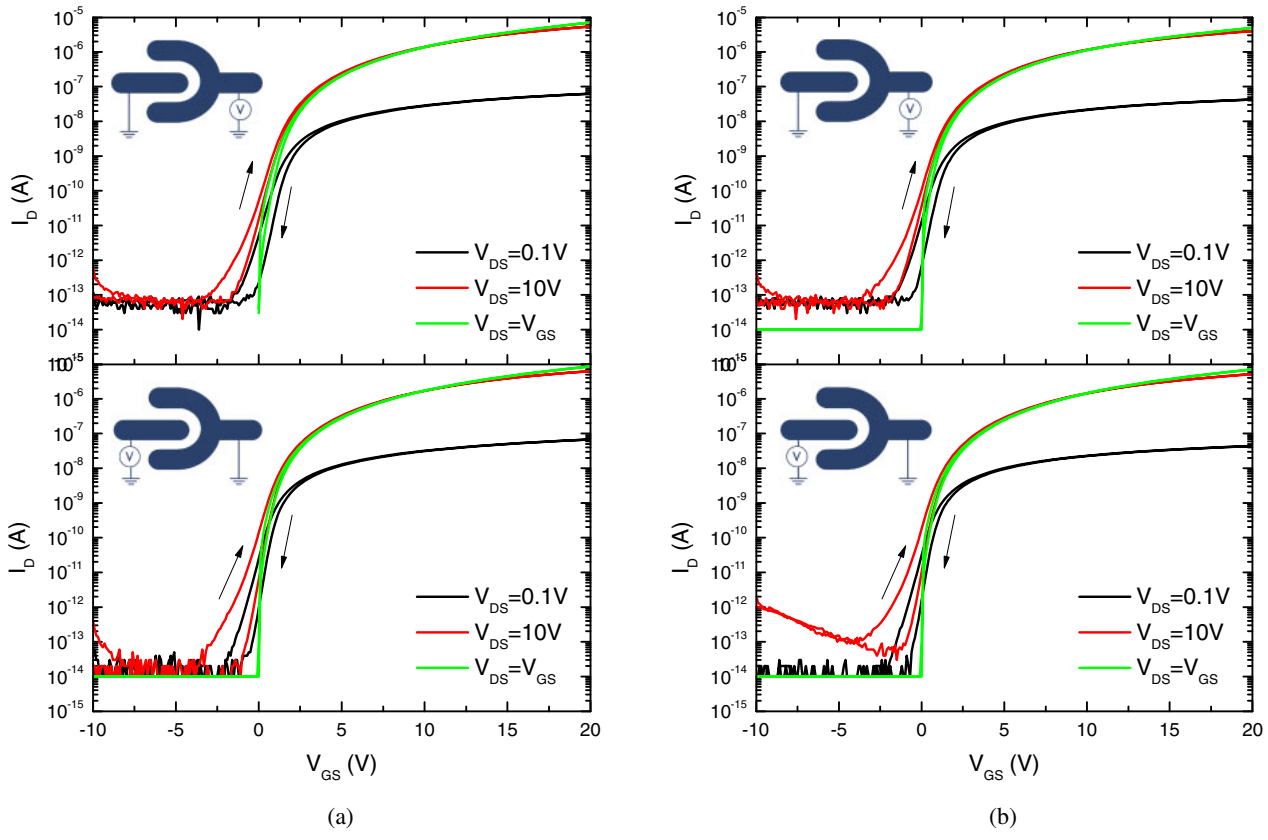


Fig. 4. (Color online) Asymmetric transfer characteristics of half Corbino a-Si:H TFT with $L = 6\,\mu m$ and $OV = 6\,\mu m$ for different source bias conditions: (a) unpatterned gate electrode and (b) patterned gate electrode.

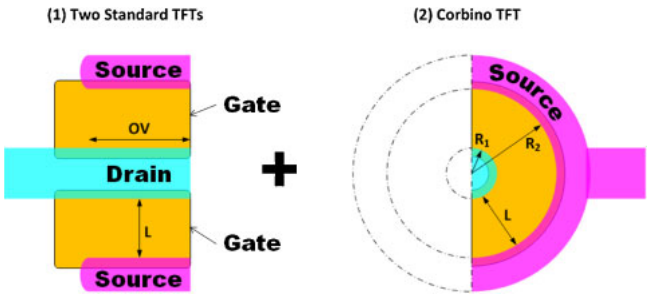


Fig. 5. (Color online) Conceptual configuration of effective channel width and length (geometric factor) definition for half-Corbino a-Si:H TFT.

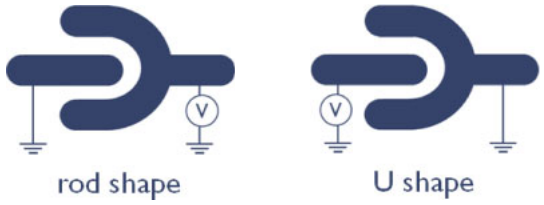


Fig. 6. (Color online) Conceptual configurations of source bias conditions for half-Corbino a-Si:H TFTs.

Half Corbino a-Si:H TFT is considered to be composed of following two parts as shown in Fig. 5; (1) two standard a-Si:H TFTs with the channel width same as overlap (OV) with the rod-shape electrode. (2) The half part of a-Si:H Corbino TFT with R_1 and R_2. Therefore, we can use the classic concept of channel width and length definition for standard TFT part (1), and the geometrical factor concept of effective channel width and length definition for Corbino TFT part (2), respectively.

Based on these definitions, we can express the drain-current (I_D) for each bias condition by using the geometrical factors of half Corbino TFT as follows:

$$I_D^{\text{Linear}} = f_{g0}\mu C_{OX}\left[(V_{GS} - V_{TH})\frac{V_{DS} - V_{DS}^2}{2}\right],$$

where

$$f_{g0} = \frac{2OV}{L} + \frac{\pi}{\ln(R_2/R_1)}, \quad (1)$$

$$I_D^{\text{Saturation}} = f_g^* \mu C_{OX}(V_{GS} - V_{TH})^2,$$

where

$$f_{g1} = \frac{1}{2} \times \left\{\frac{2OV}{L} + \frac{\pi}{\ln[6R_2'/(R_2' + 5R_1)]}\right\}, \quad (2)$$

$$f_{g2} = \frac{1}{2} \times \left\{\frac{2OV}{L} + \frac{\pi}{\ln[(9R_2 + R_1')/10R_1']}\right\}, \quad (3)$$

where f_{g1} is for source bias on U-shape electrode and f_{g2} is for source bias in rod-shape electrode. As discussed previously, the drain-current does not flow through the whole source electrode length but is rather limited to a specific length, which is the so-called TFT characteristic length (L_T)[12] located near the electrode edge. Hence, the characteristic length for each drain-bias condition can be defined as L_{T1} and L_{T2}, respectively. Therefore, if we apply the same definition to the half part of Corbino TFT, we have $R_2' = R_2 + L_{T1}$ for source bias condition (1) and $R_1' = R_1 - L_{T2}$ for the source bias condition (2).

5. Device Parameters Extraction

From TFT data shown in Figs. 3, 4, and 6, we can extract sub-threshold slope (S), threshold voltage, and field-effect mobility values. We chose the center position (at $I_D = 10^{-10}$ A) in the transfer curve of log I_D vs V_{GS}, and use the linear fitting by taking two log I_D values around the center point to extract S-value. Field-effect mobility (μ_{FE}) and threshold voltage can be calculated as follow: from the transfer curve of I_D vs V_{GS}, we chose a specific value of I_D at $V_{GS} = 15$ V. By taking 90 and 10% of this selected I_D value, we define the fitting range in I_D vs V_{GS} experimental characteristics. From the slope and x-axis intercept of the calculated curve, the field-effect mobility and threshold voltage have been extracted using different geometrical factors in eqs. (1)–(3). The maximum slope method[13] can also be used for the electrical parameter extraction, where the field-effect mobility can be calculated from transconductance maximum (g_m) and the threshold voltage is linearly extrapolated from the drain current at the transconductance peak. We have used such method in the past for a-Si:H TFTs. When compared both methods (maximum slope and one used in the paper) negligible difference in calculated mobility and threshold voltage values are observed.[11] However, some of the a-Si:H TFTs can have non-linearity in I–V curves, and transconductance peak value can be exaggerated. To prevent this possible error, we adopt the fitting range method in our paper. The fitting range must be clearly defined in order to compare data obtained from different devices. Calculated device parameters are summarized in Table I for linear (low V_{DS}) and saturation (high V_{DS}) region, respectively. Figure 6 shows the conceptual configurations of source bias conditions for half-Corbino TFTs corresponding to ones in Tables I and II.

As shown in the table, despite drain bias condition changes, the sub-threshold slope, field-effect mobility, and threshold voltage are similar for both bias conditions. Therefore, asymmetric biasing of a-Si:H half-Corbino TFT can change the ON-current characteristics while the sub-threshold slope, threshold voltage, and field-effect mobility remain the same regardless of drain bias conditions for a given device dimensions. Along with the minimized pixel (rod-shaped electrode)-to-gate capacitance (C_{GS}) compared to normal TFT, these unperturbed characteristics can be advantageous when device is used as a switching device for AM-LCDs, which will be discussed in following section.

Table I also shows the extracted electrical parameters of the a-Si:H half-Corbino TFTs with patterned gate electrode for fixed overlap (= 6 μm), and for different channel lengths (L). As shown in the table, while the sub-threshold swings of transistors for each gate electrode configuration remain same, field effect mobilities of TFTs with unpatterned gate electrode are consistently higher than those of TFTs with patterned gate electrode. Using characteristic length definition in eqs. (2) and (3), we are proposing to explain the differences in ON-current and mobility values between TFTs with patterned and unpatterned gate electrodes. Figure 3 shows that the ON-current levels of TFT with unpatterned gate is 1.23 times higher than that of TFT for patterned gate

Table I. For different source bias conditions, extracted parameters of half Corbino TFT with patterned-gate and unpatterned gate electrodes for $OV = 6\,\mu m$ and different channel lengths (L).

Unpatterned gate

Source biased Length (L)	$V_{DS} = 0.1$ V						$V_{DS} = V_{GS}$					
	Rod shape			U shape			Rod shape			U shape		
	4	6	10	4	6	10	4	6	10	4	6	10
S (mV/decade)	444	437	423	411	346	395	465	532	432	467	368	407
V_{th} (V)	2.5	2.4	3.2	2.2	1.8	2.6	2.1	1.9	2.7	2.0	1.7	2.3
μ_{FE} ($cm^2\,V^{-1}\,s^{-1}$)	0.25[a]	0.25[a]	0.25[a]	0.26[a]	0.26[a]	0.26[a]	0.54[c]	0.56[c]	0.53[c]	0.60[b]	0.57[b]	0.51[b]

Patterned gate

Source biased Length (L)	$V_{DS} = 0.1$ V						$V_{DS} = V_{GS}$					
	Rod shape			U shape			Rod shape			U shape		
	4	6	10	4	6	10	4	6	10	4	6	10
S (mV/decade)	431	428	432	469	348	451	448	510	434	515	373	457
V_{th} (V)	1.0	1.3	2.1	0.7	0.9	1.9	1.5	1.1	2.3	1.9	1.5	2.5
μ_{FE} ($cm^2\,V^{-1}\,s^{-1}$)	0.14[a]	0.17[a]	0.14[a]	0.13[a]	0.17[a]	0.14[a]	0.39[c]	0.37[c]	0.36[c]	0.46[b]	0.46[b]	0.40[b]

a) Geometrical factor f_{g0} is used to extract the parameter.
b) Geometrical factor f_{g2} is used to extract the parameter.
c) Geometrical factor f_{g1} is used to extract the parameter.

Table II. For different source bias conditions, extracted parameters of half Corbino TFT with patterned-gate and unpatterned gate electrodes for the fixed channel length ($L = 6\,\mu m$) and different overlap widths (OV).

Unpatterned gate

Source biased Overlap (OV)	$V_{DS} = 0.1$ V								$V_{DS} = V_{GS}$							
	Rod shape				U shape				Rod shape				U shape			
	0	3	6	10	0	3	6	10	0	3	6	10	0	3	6	10
S (mV/decade)	431	438	437	421	345	389	346	351	508	513	532	516	360	407	368	372
V_{th} (V)	1.4	2.3	2.4	2.2	1.9	2.2	1.8	1.8	1.7	1.9	1.9	1.7	1.8	2.1	1.7	1.8
μ_{FE} ($cm^2\,V^{-1}\,s^{-1}$)	0.21[a]	0.25[a]	0.25[a]	0.25[a]	0.27[a]	0.26[a]	0.26[a]	0.26[a]	0.53[c]	0.54[c]	0.56[c]	0.55[c]	0.56[b]	0.55[b]	0.56[b]	0.57[b]

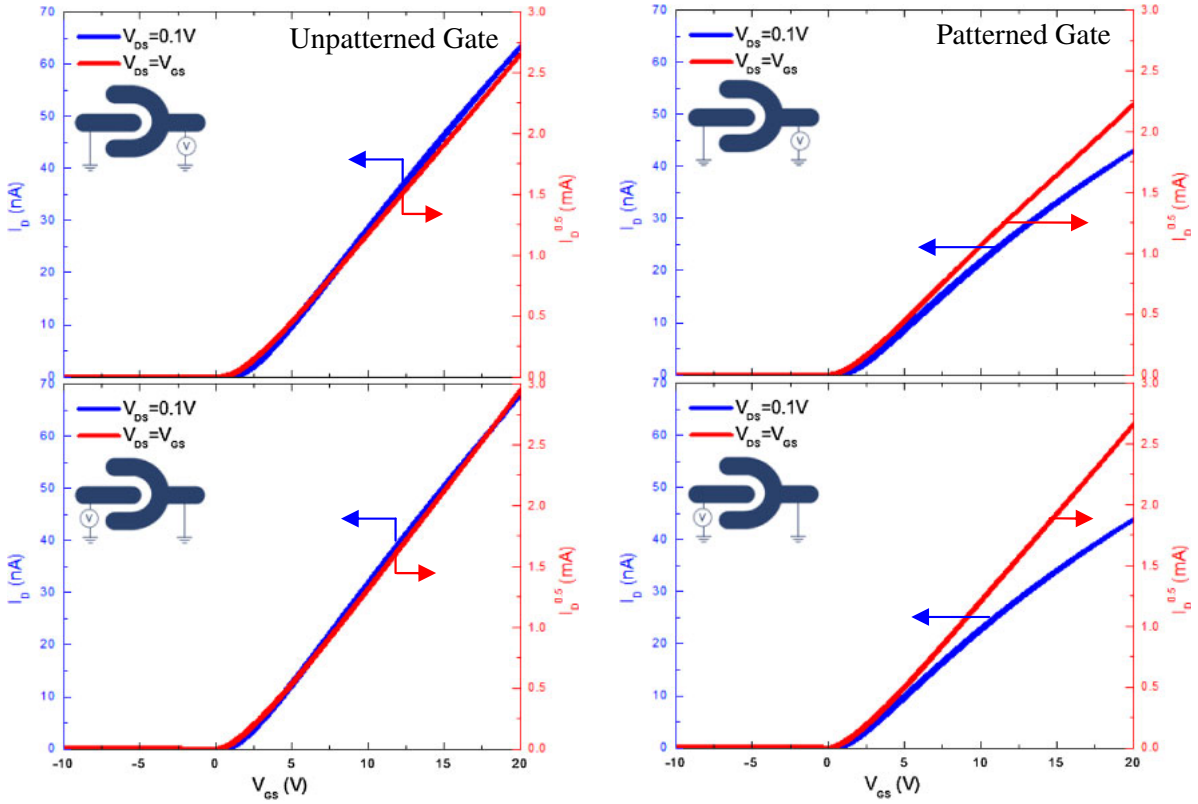
Patterned gate

Source biased Overlap (OV)	$V_{DS} = 0.1$ V								$V_{DS} = V_{GS}$							
	Rod shape				U shape				Rod shape				U shape			
	0	3	6	10	0	3	6	10	0	3	6	10	0	3	6	10
S (mV/decade)	450	402	428	410	393	343	348	333	550	503	510	512	414	365	372	341
V_{th} (V)	1	1.3	1.3	1.2	1.1	1.1	0.9	1	1.5	1.3	1.2	1.2	2.2	1.7	1.6	1.6
μ_{FE} ($cm^2\,V^{-1}\,s^{-1}$)	0.12[a]	0.16[a]	0.17[a]	0.18[a]	0.13[a]	0.17[a]	0.17[a]	0.18[a]	0.33[c]	0.36[c]	0.37[c]	0.44[c]	0.41[b]	0.44[b]	0.46[b]	0.48[b]

a) Geometrical factor f_{g0} is used to extract the parameter.
b) Geometrical factor f_{g2} is used to extract the parameter.
c) Geometrical factor f_{g1} is used to extract the parameter.

at the same bias condition. At the same time, Table I shows that field-effect mobility of TFT ($OV = 6\,\mu m$ and $L = 6\,\mu m$) with unpatterned gate is 1.21 times higher than that of TFT with patterned gate for same saturation bias condition. Since the overlap between source and patterned gate electrodes is only $1\,\mu m$, we can speculate that this overlap is not large enough in comparison to required TFT characteristic length (L_T), resulting in reduced ON-current levels and field-effect mobility values. This behavior is also clearly shown in Fig. 6. In comparison to Fig. 7(a) for unpatterned gate, Fig. 7(b) for patterned gate shows the non-linearity at high V_{GS} in the saturation regime operation, which results in smaller extracted V_{TH} value. From Table I, we can observe the V_{TH} dependence on the varying channel length (L) for each gate configuration. The V_{TH} increases as the channel length increases for both patterned and unpatterned gate devices, which is consistent with the previously reported data,[14] while the device mobility seems to be channel length independent.

We also extracted the electrical parameters of transistors with the patterned and unpatterned gate electrodes for different overlap widths, and they are summarized in Table II. Different from transistors with different channel lengths, transistors with different overlap widths do not show much difference in the extracted electrical parameters for both patterned and unpatterned gate electrodes. This observation is consistent with the previous observation that the changes in channel width of transistor do not affect the electrical properties.[15] Therefore, we can linearly control the output current of half Corbino a-Si:H TFT by chaining the overlap width while maintaining the same electrical parameters, which will be beneficial in designing circuits



(a) (b)

Fig. 7. (Color online) Asymmetric transfer characteristics of half Corbino a-Si:H TFT with $L = 6\,\mu m$ and $OV = 6\,\mu m$. Curves used for extraction of the threshold voltage and mobility are also shown: (a) unpatterned gate electrode and (b) patterned gate electrode.

with multiple transistors having different channel widths. However, here again, transistors with the patterned gate electrode show a lower threshold voltages in comparison to the ones with the unpatterned gate electrode, which we can assume is due to non-linearity of TFT characteristics. In general, we observe a larger non-linearity in current–voltage characteristics for TFT with the patterned gate.

6. Possible Applications of a-Si:H Half-Corbino TFTs to Flat Panel Displays

It is possible to use the half-Corbino a-Si:H TFT for flat-panel display applications. Figures 8(a) and 8(b) shows schematic top views and their equivalent circuit models of the half-Corbino a-Si:H TFT used as a switching TFT for conventional AM-LCDs, and as a switching and driving TFT for AM-OLEDs, respectively. The storage capacitor is not taken into consideration in these simple pixel-electrode schematics. When the device is used as a switching TFT, half-Corbino TFT has an advantage of having a much smaller parasitic gate-to-source capacitance (C_{GS}) than a standard TFT.[4] For example, let us assume we have a standard TFT that has channel width of 30 and $2\,\mu m$ overlap between source and gate electrode. If we replace this TFT with a half Corbino TFT that has the same channel length and overlap, the area corresponding to C_{GS} will be reduced from 60 to $50\,\mu m^2$, which is 17% reduction. If we use the half Corbino TFT with the patterned gate, this area is even further reduced to $36\,\mu m^2$, which is 40% reduction. This reduction will minimize pixel-voltage drop value (error voltage):[16]

$$\Delta V_p = \frac{C_{GS}(V_{GH} - V_{GL})}{C_{GS} + C_{LC} + C_{ST} + C_G}, \tag{4}$$

where V_{GH} is switch turn-on gate voltage, V_{GL} is switch turn-off gate voltage, C_{LC} is capacitance of LC, C_{ST} is storage capacitance, and C_{GS} is gate-to-channel capacitance. A low error voltage will reduce the flicker and sticking image defects[17] and as a result, the quality of the a-Si:H TFT AM-LCD is expected to improve. In the AM-LCD driving scheme, the polarity of the data line bias changes from line to line with respect to the common line-inversion method. Hence, the positions of drain and source in the TFT should be opposite in odd and even data lines. In such a case, as mentioned above, half-Corbino TFTs in the active-matrix array will have different ON-current but same OFF current values for different lines. Since the ON current is only used for charging the storage capacitor, the asymmetric ON current will not influence the storage capacitor voltage as long as the switch turn-on time is long enough. Since the TFT switch turn-off time is relatively very long compared with the switch-on time in the AM-LCD operation, the symmetric OFF-current behavior of the half-Corbino a-Si:H TFT regardless of the bias condition can make this device the optimum switching device for AM-LCDs.

In AM-LCD, the dynamic power consumption of one pixel of the active-matrix array backplane can be expressed as follows:

$$\text{Power} = f C_{\text{Total}} V_{DS}^2 \tag{5}$$

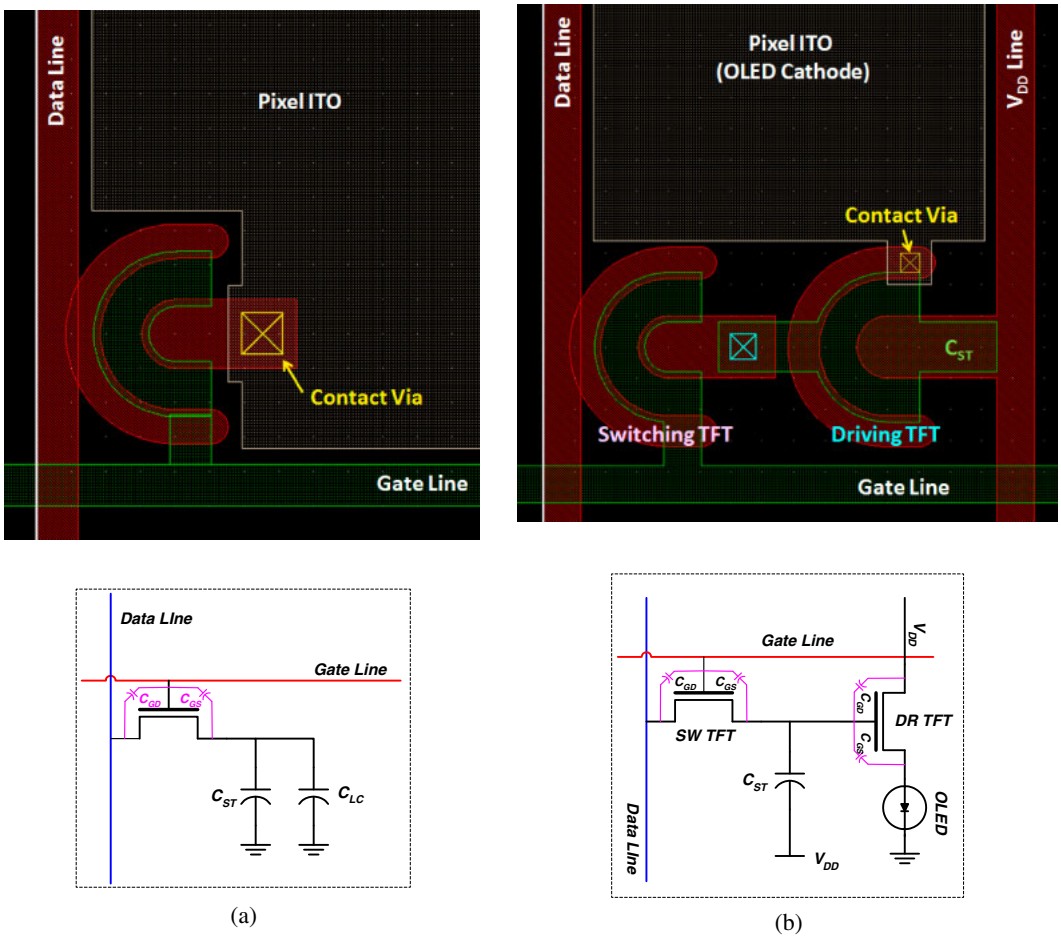


Fig. 8. (Color online) Top views and their equivalent circuits of the proposed half-Corbino a-Si:H TFT pixel circuits for (a) AM-LCD and (b) AM-OLED.

where f is the display driving frequency, and C_{Total} is sum of C_{GS}, C_{GD}, C_{G}, C_{ST}, and C_{LC}. In general, the frame frequency, C_{ST}, and C_{LC} are fixed values in AM-LCD operation. To minimize the pixel error voltage shown in eq. (4), the storage capacitor (C_{ST}) is generally chosen as large as C_{LC} or even two times larger, resulting in the unnecessary power consumption. For half Corbino a-Si:H TFT, since the parasitic capacitance is reduced in comparison to standard TFT, the storage capacitor can be reduced to maintain the same pixel error voltage level resulting in a lower value of the total capacitance of switching TFT. Therefore, for a certain gray level (a fixed drain bias), the power consumption of each pixel can be linearly reduced resulting in better power efficiency and enhanced the pixel aperture ratio due to the reduction of storage capacitor.

By changing the device bias condition, ON-current of half-Corbino TFT can be increased, and TFT can also be used as driving transistor in AM-OLED where simple pixel circuit electrode requires at least two transistors. At the same time, TFT with unpatterned gate electrode can be used to boost ON-current level in comparison to TFT with patterned gate electrode. Figure 8(b) shows an example of top view and its equivalent circuit of AM-OLED pixel electrode circuit. By using the half-Corbino TFT as a switching transistor in AM-OLED, the power consumption will be expressed by eq. (5) during the programming stage.[18] Therefore, the power consumption will be reduced since the programmed gate voltage variation is caused by the feed-through effect of C_{GS}.[19] During the driving state, the power consumption becomes a static model due to the DC bias (V_{DD}) on the driving transistor, and it can be defined as $P_{\mathrm{TFT}} = V_{\mathrm{DD}}^2/R_{\mathrm{TFT}}$ where R_{TFT} is the channel resistance determined by V_{GS} (gate node voltage defined at the programming stage). Therefore, in order to reduce the V_{DD} level, we need to use a transistor with a large channel width (W/L can be large). Considering that the channel length is usually fixed value in the current a-Si:H technology, the channel width needs to be increased to achieve the power reduction. Using half-Corbino geometry, we can achieve a larger W/L.[11] At the same time, as reported for a-Si:H Corbino TFT,[20] we are expecting an enhanced electrical stability of half-Corbino a-Si:H TFT.

In addition, by using half-Corbino a-Si:H TFT configuration, we can avoid unnecessary processing step to define the source/drain electrodes which are required in Corbino a-Si:H TFT configuration. Due to its unique geometry, inner circle electrode needs an extra mask step to realize the connection to the signal line. In half-Corbino a-Si:H TFT configuration, the source and drain electrode can be defined at the same time without extra mask and process step.

Finally, so far the patterned half-Corbino TFT configuration has not been used in a practical panel design due to expected alignment tolerance problem where conventional photo-lithography system is used. This can result in non-uniformity during device fabrication over large area. However, if alignment tolerance can be reduced ($<0.01\,\mu$m)

by using the latest photo-lithography system, the patterned half-Corbino configuration can be implemented in near future for large size panel displays.

7. Conclusions

We have fabricated two types of half-Corbino a-Si:H TFTs: one with patterned and one with unpatterned gate electrode. We investigated their electrical characteristics under different drain bias conditions. Due to unique half annular device geometry, when source is connected to outer U-shaped electrode, ON-current is about 1.2 times higher than when source is applied to outer U-shape electrode at high drain voltages (>10 V) while OFF-current remains 0.1 pA for both conditions. The sub-threshold swing is small for both cases, while threshold voltage and field-effect mobility show small difference for each case.

Thanks to its stable bi-directional OFF-current as well as a even lower gate-to-pixel capacitance when the patterned gate electrode is used, a-Si:H Half-Corbino TFT appears to be an excellent candidate as a switching TFT for AM-LCDs in comparison to standard a-Si:H TFT. We also found that the a-Si:H half-Corbino TFT can be an adequate device to be used as a switching and driving TFT for AM-OLEDs.

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